UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/019,407	03/25/2002	Yoshinobu Kimura	520.41003 X00	3893

20457 7590 04/08/2004

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-9889

EXAMINER	
SCHILLINGER, LAURA M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/019,407	KIMURA ET AL..	
	Examiner	Art Unit	
	Laura M Schillinger	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/28/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6, 10-11, 16-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al ('730).

Yamazaki teaches the following claim limitations as cited below:

1.A polycrystalline semiconductor thin film substrate an insulative substrate and a polycrystalline semiconductor thin film formed on one surface of the insulative substrate, wherein in which the number of crystal grains the number of closest crystal grains of 6 is greatest among plural crystal grains that form the polycrystalline semiconductor thin film (Col.8 ,lines: 25-45 and Fig.2A).

2. A polycrystalline semiconductor thin film substrate as defined in claim 1, wherein the roughness of the grain boundaries on the surface of the polycrystalline semiconductor thin film is 5 nm or less (Col.6, lines: 5-10).

3. A semiconductor device comprising plural transistors formed in a polycrystalline semiconductor thin film, wherein the number of crystal grains with the number of closest crystal grains of 6 is greatest among plural crystal grains that form the polycrystalline semiconductor thin film(Col.8 ,lines: 25-45 and Fig.2A).

4. A semiconductor device as defined in claim 3, wherein the roughness of the grain the polycrystalline boundaries on the surface of semiconductor thin film is 5 nm or less(Col.6, lines: 5-10)..

5. A semiconductor device comprising plural transistors formed in a polycrystalline semiconductor thin film, wherein a square region with a 10 um side and in which 50 to 100% of the crystal grains have the number of closest crystalline grains of 6 is present so as to include the semiconductor thin film in the polycrystalline semiconductor thin film(Col.8 ,lines: 25-45 and Fig.2A).

6. A semiconductor device as defined in claim wherein the roughness of the grain boundaries on the surface of the polycrystalline semiconductor thin film is 5 nm or less(Col.6, lines: 5-10)..

10. An electronic apparatus comprising a semiconductor device in which plural transistors are formed polycrystalline semiconductor thin film wherein a square region with a 10 um side and 50 to 100% of the crystal grains have the 6 is present so as to include the center of the polycrystalline semiconductor thin film in the polycrystalline semiconductor thin film(Col.8 ,lines: 25-45 and Fig.2A).

11. An electronic apparatus as defined in claim 10, wherein the roughness of the grain boundaries on the surface of the polycrystalline semiconductor thin film is 5 nm or less(Col.6, lines: 5-10)..

12. An electronic apparatus as defined in claim 7, wherein the electronic apparatus is a liquid crystal display, the semiconductor device has transistors for operating each of pixels a liquid crystal display panel and transistors constituting peripheral driver circuitries and is stacked and attached on the liquid crystal display panel of the liquid crystal display (Col.24, lines: 60-65).

13An electronic apparatus as defined wherein the electronic device is a data processor, and a central processing unit, a cash circuitry, a memory circuitry, a peripheral circuitry, an input/output circuitry and a bus circuitry are formed with each of the transistors of the in claim semiconductor device (Fig.16C).

16. A semiconductor device in which a transistor is formed in a polycrystalline semiconductor thin film wherein the number of crystal grains with the number of closest crystal grains of 6 greatest among plural crystal grains forming the channel region of the transistor(Col.8 ,lines: 25-45 and Fig.2A).

17. A semiconductor device in which plural transistors are formed in the polycrystalline semiconductor thin film wherein a square region with a 10 um side and in which 50 to 100% of the crystal grains have the number of closest crystalline grains of 6 present so as to include the center of the polycrystalline semiconductor thin film in the polycrystalline semiconductor thin film(Col.8 ,lines: 25-45 and Fig.2A).

18. A semiconductor device as wherein the roughness of the defined in claim grain boundaries on the surface of the polycrystalline semiconductor thin film is 5 nm or less(Col.6, lines: 5-10).

19.An electronic apparatus having plural transistors formed in a polycrystalline semiconductor thin film, wherein the number of crystal grains with the number of closest crystal grains of 6 is greatest among plural crystal grains forming the polycrystalline semiconductor thin film(Col.8 ,lines: 25-45 and Fig.2A).

20. An electronic apparatus as defined in claim 19, wherein the roughness of the grain boundaries on the surface of the polycrystalline semiconductor thin film is 5 nm or less(Col.6, lines: 5-10).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by Kusumoto ('102).

7. Kusumoto teaches an electronic apparatus comprising a semiconductor device with plural transistors formed in a polycrystalline silicon thin film, wherein variation in the threshold voltage is 0.1 V or less (Col.12, lines: 30-35).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8-9, 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kusumoto ('102) as applied to claim 7 above, and further in view of Yamazaki et al (('730).

Kusumoto teaches a transistor with threshold voltage fluctuations of 0.1 V, by implementing a silicon transistor, however fails to teach that the active region is a hexagonal

silicon transistor with a smooth grain surface which may be applied in various applications as claimed by the Applicant.

However, Yamazaki teaches the following claimed limitations:

8. An electronic apparatus as defined in claim 7, wherein the number of crystal grains with the number of closest crystal grain of 6 is greatest among plural crystal grains that form the polycrystalline semiconductor thin film(Col.8 ,lines: 25-45 and Fig.2A).

9. An electronic apparatus as defined in claim 8, wherein the roughness of the grain boundaries on the surface of the polycrystalline semiconductor thin film is 5 nm or less (Col.6, lines: 5-10).

12. An electronic apparatus as defined in claim 7, wherein the electronic apparatus is a liquid crystal display, the semiconductor device has transistors for operating each of pixels a liquid crystal display panel and transistors constituting peripheral driver circuitries and is stacked and attached on the liquid crystal display panel of the liquid crystal display (Col.24, lines: 60-65).

13. An electronic apparatus as defined wherein the electronic device is a data processor, and a central processing unit, a cash circuitry, a memory circuitry, a peripheral circuitry, an input/output circuitry and a bus circuitry are formed with each of the transistors of the in claim semiconductor device (Fig.16C).

It would have been obvious to one of ordinary skill in the art to modify Kusumoto's transistor to include a smooth hexagonal grain structure as taught by Yamazaki in the various known

applications for transistors disclosed by Yamazaki because as Yamazaki teaches such a crystalline structure allows for a superior path of electron flow (Col.2, lines:5-15) as a result of the lack of crystalline defects (Col.4, lines: 15-20).

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter: .

In reference to claims 14 and 15, Yamazaki teaches a method of manufacturing a polycrystalline semiconductor thin film substrate by forming an amorphous semiconductor thin film (104) on the surface of an insulative substrate (101), then irradiating the amorphous semiconductor film with a laser beam thereby to crystallize the amorphous semiconductor film and forming a polycrystalline semiconductor thin film (Col.9, lines: 20-25), wherein the method comprises irradiating the rear face of the insulative substrate or the amorphous semiconductor film with a UV-ray thereby to heat the amorphous semiconductor film melting temperature or lower (Col.9, lines: 30-35), and repeatedly irradiating the surface of the amorphous semiconductor film with a laser beam at a suitable shape selection laser energy density Ec to form greatest number of crystal grains with the number of closest crystal grains of 6 (Col.8 ,lines: 25-45 and Fig.2A),

However, Yamazaki fails to teach nor suggest synchronizing the period of the laser beam irradiation and the period of the UV-ray heating, and dividing, by an optical component, the laser beam into two optical channels with the optical length of one of them being made longer such that it reaches the laser beam irradiation position with a delay, thereby forming the polycrystalline semiconductor thin film.

In reference to claim 15, Yamazaki fails to teach a method of manufacturing a polycrystalline semiconductor thin film substrate as defined in claim 14, wherein one of the laser beams divided into two optical channels that passes through a channel of a shorter optical wavelength is attenuated by being passed through an optical attenuator and caused to reach the laser beam irradiation position, thereby forming the polycrystalline semiconductor thin film.

Gopalakishnan ('127) teaches an optical modulator wherein one of the laser beams divided into two optical channels that passes through a channel of a shorter optical wavelength is attenuated by being passed through an optical attenuator (Fig.3 (λ_1 and λ_2), however fails to teach to use the modulated laser in application of crystallizing a polysilicon layer. Therefore claims 14 and 15 both contain allowable subject matter.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMS

4/2/04